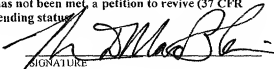


JC17 Rec'd PGT/PTO 14 MAY 2001

FORM PTO-1390 (REV. 11-2000)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTORNEY'S DOCKET NUMBER 9138-0018	
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371				U.S. APPLICATION NO. (if known, see 37 CFR 1.5) 09/831812	
INTERNATIONAL APPLICATION NO. PCT/US99/26698		INTERNATIONAL FILING DATE 12 Nov. 1999 (12.11.99)		PRIORITY DATE CLAIMED 13.11.98	
TITLE OF INVENTION OSCILLATORY NEUROCOMPUTERS WITH DYNAMIC CONNECTIVITY					
APPLICANT(S) FOR DO/EO/US <u>Frank C. Hoppensteadt, et al.</u>					
Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:					
1. <input checked="" type="checkbox"/> This is a FIRST submission of items concerning a filing under 35 U.S.C. 371. 2. <input type="checkbox"/> This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. 371. 3. <input checked="" type="checkbox"/> This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below. 4. <input type="checkbox"/> The US has been elected by the expiration of 19 months from the priority date (Article 31). 5. <input checked="" type="checkbox"/> The copy of the International Application as filed (35 U.S.C. 371(c)(2)) a. <input type="checkbox"/> is attached hereto (required only if not communicated by the International Bureau). b. <input checked="" type="checkbox"/> has been communicated by the International Bureau. c. <input checked="" type="checkbox"/> is not required, as the application was filed in the United States Receiving Office (RO/US). 6. <input type="checkbox"/> An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)). a. <input type="checkbox"/> is attached hereto. b. <input type="checkbox"/> has been previously submitted under 35 U.S.C. 154(d)(4). 7. <input type="checkbox"/> Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)) a. <input type="checkbox"/> are attached hereto (required only if not communicated by the International Bureau). b. <input type="checkbox"/> have been communicated by the International Bureau. c. <input type="checkbox"/> have not been made; however, the time limit for making such amendments has NOT expired. d. <input type="checkbox"/> have not been made and will not be made. 8. <input type="checkbox"/> An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)). 9. <input type="checkbox"/> An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)). 10. <input type="checkbox"/> An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)). Items 11 to 20 below concern document(s) or information included: 11. <input type="checkbox"/> An Information Disclosure Statement under 37 CFR 1.97 and 1.98. 12. <input type="checkbox"/> An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included. 13. <input checked="" type="checkbox"/> A FIRST preliminary amendment. 14. <input type="checkbox"/> A SECOND or SUBSEQUENT preliminary amendment. 15. <input type="checkbox"/> A substitute specification. 16. <input type="checkbox"/> A change of power of attorney and/or address letter. 17. <input type="checkbox"/> A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825. 18. <input type="checkbox"/> A second copy of the published international application under 35 U.S.C. 154(d)(4). 19. <input type="checkbox"/> A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4). 20. <input type="checkbox"/> Other items or information:					

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U.S. APPLICATION NO. 099,831,812 INTERNATIONAL APPLICATION NO. PCT/US99/26698	ATTORNEY'S DOCKET NUMBER 9138-0018
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<p>21. <input checked="" type="checkbox"/> The following fees are submitted:</p> <p>BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)):</p> <p>Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO. \$1000.00</p> <p>International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO. \$860.00</p> <p>International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO. \$710.00</p> <p>International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4). \$690.00</p> <p>International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4). \$100.00</p> <p style="text-align: center;">ENTER APPROPRIATE BASIC FEE AMOUNT =</p> <p>Surcharge of \$130.00 for furnishing the oath or declaration later than months from the earliest claimed priority date (37 CFR 1.492(e)). <input type="checkbox"/> 20 <input type="checkbox"/> 30</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 20%;">CLAIMS</th> <th style="width: 20%;">NUMBER FILED</th> <th style="width: 20%;">NUMBER EXTRA</th> <th style="width: 20%;">RATE</th> <th style="width: 20%;">\$</th> </tr> </thead> <tbody> <tr> <td>Total claims</td> <td>19 - 20 =</td> <td></td> <td>x \$18.00</td> <td>\$ 0.00</td> </tr> <tr> <td>Independent claims</td> <td>1 - 3 =</td> <td>4</td> <td>x \$80.00</td> <td>\$ 320.00</td> </tr> <tr> <td colspan="4">MULTIPLE DEPENDENT CLAIM(S) (if applicable)</td> <td>+ \$270.00</td> </tr> <tr> <td colspan="4" style="text-align: right;">TOTAL OF ABOVE CALCULATIONS =</td> <td>\$ 320.00</td> </tr> <tr> <td colspan="4"> <input checked="" type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2. </td> <td>\$ 160.00</td> </tr> <tr> <td colspan="4" style="text-align: right;">SUBTOTAL =</td> <td>\$ 160.00</td> </tr> <tr> <td colspan="4">Processing fee of \$130.00 for furnishing the English translation later than months from the earliest claimed priority date (37 CFR 1.492(f)).</td> <td>\$</td> </tr> <tr> <td colspan="4" style="text-align: right;">TOTAL NATIONAL FEE =</td> <td>\$</td> </tr> <tr> <td colspan="4">Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). \$40.00 per property +</td> <td>\$</td> </tr> <tr> <td colspan="4" style="text-align: right;">TOTAL FEES ENCLOSED =</td> <td>\$ 260.00</td> </tr> <tr> <td colspan="4"></td> <td style="text-align: right;">Amount to be refunded: \$</td> </tr> <tr> <td colspan="4"></td> <td style="text-align: right;">charged: \$</td> </tr> </tbody></table> <p>a. <input checked="" type="checkbox"/> A check in the amount of \$ <u>260.00</u> to cover the above fees is enclosed.</p> <p>b. <input type="checkbox"/> Please charge my Deposit Account No. _____ in the amount of \$ _____ to cover the above fees. A duplicate copy of this sheet is enclosed.</p> <p>c. <input checked="" type="checkbox"/> The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. <u>07-0135</u>. A duplicate copy of this sheet is enclosed.</p> <p>d. <input type="checkbox"/> Fees are to be charged to a credit card. WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.</p> <p>NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137 (a) or (b)) must be filed and granted to restore the application to pending status.</p> <p>SEND ALL CORRESPONDENCE TO Gallagher & Kennedy, P.A. 2575 E. Camelback Road Phoenix, Arizona 85016-9225</p> <p style="text-align: right;">  SIGNATURE <u>Thomas D. MacBlain</u> NAME <u>24, 583</u> REGISTRATION NUMBER </p>	CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	\$	Total claims	19 - 20 =		x \$18.00	\$ 0.00	Independent claims	1 - 3 =	4	x \$80.00	\$ 320.00	MULTIPLE DEPENDENT CLAIM(S) (if applicable)				+ \$270.00	TOTAL OF ABOVE CALCULATIONS =				\$ 320.00	<input checked="" type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.				\$ 160.00	SUBTOTAL =				\$ 160.00	Processing fee of \$130.00 for furnishing the English translation later than months from the earliest claimed priority date (37 CFR 1.492(f)).				\$	TOTAL NATIONAL FEE =				\$	Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). \$40.00 per property +				\$	TOTAL FEES ENCLOSED =				\$ 260.00					Amount to be refunded: \$					charged: \$
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: : Date: May 14, 2001

Frank C. Hoppensteadt et al. : Group Art Unit: Unassigned

Serial No.: Not yet assigned (PCT/US99/26698) : Examiner: Unassigned

Filed: Herewith (13 Nov. 1998 – Priority
Date Claimed) :
(12 Nov. 1999 – Int'l
Filing Date) :

Title: OSCILLATORY NEUROCOMPUTERS WITH DYNAMIC CONNECTIVITY

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
BOX PCT
Washington, D.C. 20231

Sir/Madam:

This preliminary amendment is being submitted to further claim applicants' invention.

Please amend the above-identified patent application as follows:

In the Specification:

Please replace the sentence on page 5, lines 20-21, with the following rewritten sentence:

-- Neurocomputer 50 comprises a finite number n (in this case, n=5) of oscillatory neural processing elements 60A, 60B, 60C, 60D, and 60E.--

Please replace the sentence on page 9, lines 5-10, with the following rewritten sentence:

-- The following formula may be used to determine the capture-range.

$$f_c = 1/(2 \bullet \pi) \bullet \sqrt{((2 \bullet \pi \bullet f_L)/(3.6 \bullet 1000 \bullet C2))} \quad (ii)$$

where C2 is the capacitance of the similarly designated capacitor in FIG. 4 and f_L is the lock-range.--

Please replace the sentence on page 9, lines 11-12, with the following rewritten sentence:

--By evaluating the formula for the capture range, one can see that the capture range is limited by the low pass filter time constant.--

Please replace the sentence on page 10, lines 4-8, with the following rewritten sentence:

--In order to implement the multiplication operation as shown by the multiplication circle 171 or 173, one should understand the following theory:

$$\cos(\omega c) \cos(\omega m) = (1/2) \bullet [\cos(\omega c - \omega m) + \cos(\omega c + \omega m)]$$

\Rightarrow Fourier Transform \Rightarrow

$$(1/4) \bullet [\delta(f + (fc - fm)) + \delta(f + (fc + fm)) + \delta(f - (fc - fm)) + \delta(f - (fc + fm))].--$$

Please replace the sentence on page 17, lines 7-8, with the following rewritten sentence:

--Let us apply the external input $a(t)$ with $c_v = c_v^0 e^{j\omega t}$ for a certain period of time.--

In the Claims:

Please cancel claim 1 without prejudice.

Please cancel claim 2 without prejudice.

Please cancel claim 3 without prejudice.

Please cancel claim 4 without prejudice.

6.(Amended) A neurocomputer comprising:

a plurality of n processing element means;

a plurality of no more than n connectors operably coupled with said
element means;

means for simultaneously applying an oscillatory signal to each of said
element means via said connectors; and

means for generating said oscillatory signal operably coupled with said
means for applying.

7.(Amended) The neurocomputer of claim 6, wherein:

each of said connectors is operably coupled with a corresponding one of said element
means.

Please cancel claim 13 without prejudice.

Please cancel claim 14 without prejudice.

25.(Amended) In a neurocomputer, a number n of active elements and a medium having no
more than n connections operably coupled to each of the active elements for application of an
input signal thereto, said active elements being phase locked loop oscillators.

REMARKS

Claims 5-12 and 15-25 remain in the application. By this amendment claims 6, 7, and
25 have been amended and claims 1-4, 13, and 14 have been canceled without prejudice.

The specification has been amended to correct various typographical and grammatical
errors contained therein.

Attached hereto is a marked-up version of the changes made to the specification and
claims by the current amendment. The attached page is captioned **“Version with markings to
show changes made.”**

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

In view of all of the above, it is believed that applicants' claims are believed allowable, and the case is now in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

GALLAGHER & KENNEDY, P.A.

Dated: 5/14/01

By: 

Thomas D. MacBlain, Reg. No. 24,583
Attorney for Applicants
2575 East Camelback Road
Phoenix, Arizona 85016
Telephone: (602) 530-8000

Title: OSCILLATORY NEUROCOMPUTERS WITH DYNAMIC
CONNECTIVITY
Preliminary Amendment
Page 5

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the specification:

The sentence on page 5, lines 20-21, has been amended as follows:

-- Neurocomputer 50 comprises a finite number n (in this case, n=5) of oscillatory neural processing elements 60A, 60B, 60C, 60D, and 60E.--

The sentence on page 9, lines 6-10, has been amended as follows:

-- The following formula may be used to determine the capture-range.

$$f_c = 1/(2 \bullet \pi) \bullet \sqrt{((2 \bullet \pi \bullet f_L)/(3.6 \bullet 1000 \bullet C_2))} \quad (ii)$$

where C₂ is the capacitance of the similarly designated capacitor in FIG. [5] 4 and f_L is the lock-range.—

The sentence on page 9, lines 11-12, has been amended as follows:

--By evaluating the formula for the capture range, one can see that the capture range is limited by the low pass filter time constant.—

The sentence on page 10, lines 4-8, has been amended as follows:

--In order to implement the multiplication operation as shown by the multiplication circle 171 or [172] 173, one should understand the following theory:

$$\cos(\omega c) \cos(\omega m) = (1/2) \bullet [\cos(\omega c - \omega m) + \cos(\omega c + \omega m)]$$

$$\Rightarrow \text{Fourier Transform} \Rightarrow$$

$$(1/4) \bullet [\delta(f + (fc - fm)) + \delta(f + (fc + fm)) + \delta(f - (fc - fm)) + \delta(f - (fc + fm))].—$$

The sentence on page 17, lines 7-8, has been amended as follows:

--Let us apply the external input a(t) with $c_{ij} = c_{ij}^0 c_j^0$ [with] for a certain period of time.--

In the claims:

Claims 1-4 have been canceled without prejudice.

6.(Amended) A neurocomputer comprising:

a plurality of n processing element means;

a plurality of no more than n connectors operably coupled with said

element means;

means for simultaneously applying an oscillatory signal to each of said

element means via said connectors; and

means for generating said oscillatory signal operably coupled with said

means for applying.

7.(Amended) The neurocomputer of claim 6, wherein:

[said plurality of connectors comprises n connectors,] each of said connectors

[being] is operably coupled with a corresponding one of said element means.

Claims 13 and 14 have been canceled without prejudice.

25.(Amended) In a neurocomputer, a number n of active elements and a medium having no more than n connections operably coupled to each of the active elements for application of an input signal thereto, said active elements being phase locked loop oscillators.

OSCILLATORY NEUROCOMPUTERS WITH DYNAMIC CONNECTIVITY

5

The present application claims priority rights based on U.S. Provisional Application Serial No. 60/108,353 filed November 13, 1998.

FIELD OF THE INVENTION

10 The present invention relates generally to computational devices and more particularly to a neural network computer requiring a minimal number of connective devices between processing elements.

BACKGROUND OF THE INVENTION

Artificial neural networks, or neurocomputers, are biologically inspired; that is, they are composed of elements that perform in a manner analogous to the most elementary functions of the biological neuron. Typically, a neurocomputer is composed of a number (n) of processing elements that may be switches or nonlinear amplifiers.

20 These elements are then organized in a way that may be related to the anatomy of the brain. The configuration of connections, and thus communication routes, between these elements represents the manner in which the neurocomputer will function, analogous to that of a program performed by digital computers. Despite this superficial resemblance, artificial neural networks exhibit a surprising number of the brain's characteristics. For

25 example, they learn from experience, generalize from previous examples to new ones, and abstract essential characteristics from inputs containing irrelevant data. Unlike a von Neumann computer, the neurocomputer does not execute a list of commands (a

program). Rather, the neurocomputer performs pattern recognition and associative recall via self-organization of connections between elements.

Artificial neural networks can modify their behavior in response to their environment. Shown a set of inputs (perhaps with desired outputs), they self-adjust to produce consistent responses. A network is trained so that application of a set of inputs produces the desired (or at least consistent) set of outputs. Each such input (or output) set is referred to as a vector. Training is accomplished by sequentially applying input vectors, while adjusting network weights according to a predetermined procedure. During training, the network weights gradually converge to values such that each input vector produces the desired output vector.

Because of their ability to simulate the apparently oscillatory nature of brain neurons, oscillatory neurocomputers are among the more promising types of neurocomputers. Simply stated, the elements of an oscillatory neurocomputer consist of oscillators rather than amplifiers or switches. Oscillators are mechanical, chemical or electronic devices that are described by an oscillatory signal (periodic, quasi-periodic, almost periodic function, etc.). Usually the output is a scalar function of the form $V(\omega t + \phi)$ where V is a fixed wave form (sinusoid, saw-tooth or square wave), ω is the frequency of oscillation, and ϕ is the phase deviation (lag or lead).

Recurrent neural networks have feedback paths from their outputs back to their inputs. As such, the response of such networks is dynamic in that after applying a new input, the output is calculated and fed back to modify the input. The output is then recalculated, and the process is repeated again and again. Ideally, successive iterations produce smaller and smaller output changes until eventually the outputs become constant. To properly exhibit associative and recognition properties, neural networks,

such as is required by Hopfield's network, must have a fully connected synaptic matrix. That is, to function optimally, recurrent network processing elements must communicate data to each other. Although some prototypes have been built, the commercial manufacture of such neurocomputers faces a major problem: A conventional recurrent neurocomputer consisting of n processing elements requires n^2 connective junctions to be fully effective. The terms connector or connective junction, as used herein throughout, are defined as a connective element that enables one processing element to receive as input data output data produced by itself or any other one processing element. For large n this is difficult and expensive.

Accordingly, a need exists for a neurocomputer with fully recurrent capabilities and requiring a minimal number of connective devices between processing elements.

SUMMARY OF THE INVENTION

In accordance with the present invention, a neurocomputer is disclosed that exhibits pattern recognition and associative recall capabilities while requiring only n connective junctions for every n processing elements employed thereby.

In a preferred embodiment of the invention, the neurocomputer comprises n oscillating processing elements that can communicate through a common medium so that there are required only n connective junctions. A rhythmic external forcing input modulates the oscillatory frequency of the medium which, in turn, is imparted to the oscillators. Any two oscillators oscillating at different frequencies may communicate provided that the input's power spectrum includes the frequency equal to the difference between the frequencies of the two oscillators in question. Thus, selective communication, or dynamic connectivity, between different neurocomputer oscillators occurs due to frequency modulation of the medium by external forcing.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a schematic diagram of a prior art recurrent neural network employing five neural processing elements.

5 FIG. 2 is a schematic diagram of a neural network according to principles of the present invention and employing five neural processing elements.

FIG. 3 is a diagrammatic illustration of results obtained through simulation of the neurocomputer according to principles of the present invention using a phase deviation model and Hebbian learning rule with parameters: $n = 60$, $t \in [0, 10]$.

10 FIG. 4 is a schematic block diagram of a phase-locked loop.

FIG. 5 is a diagrammatic illustration of the relationship between demodulated output voltage and input frequency and phase of a phase-locked loop as depicted in FIG. 4.

15 FIG. 6 is a schematic block diagram of a neural network according to principles of the present invention employing two phase-locked loops as depicted in FIG. 4.

FIG. 7 is a diagrammatic illustration of one frequency multiplication performed in the neural network depicted in FIG. 6.

FIG. 8 is a schematic diagram showing the circuit components of the neural network of FIG. 6 according to principles of the present invention.

20 FIG. 9 is a schematic block diagram of a five-oscillator neural network with associated function generator and oscilloscopes connected for testing.

FIGS. 10A-10E are oscilloscope traces of the oscillator responses of the network of FIG. 9 with a signal $\sin t$ impressed on the input.

FIGS. 11A-11E are oscilloscope traces of the oscillator responses of the network of FIG. 9 with a signal $\sin 2t$ impressed on the input.

5 FIGS. 12A-12E are oscilloscope traces of the oscillator responses of the network of FIG. 9 with a signal $\sin 3t$ impressed on the input.

FIGS. 13A-13E are oscilloscope traces of the oscillator responses of the network of FIG. 9 with a signal $\sin 10t$ impressed on the input.

DESCRIPTION OF THE PREFERRED EMBODIMENT

10 FIG. 1 schematically illustrates a conventional recurrent neurocomputer 10 comprising n (in this case, $n=5$) neural processing elements 20. Elements 20 may comprise switches, amplifiers, oscillators or any other suitable neurocomputer element type known in the art. In order for each of elements 20 to communicate with the others
15 of elements 20, neurocomputer 10 necessarily includes n^2 (in this case, $n^2=25$) connective junctions 30 to which conductors 40 are attached. As can be observed, where the number n of elements 20 grows large, the implementation of such a neurocomputer becomes prohibitively difficult, from both cost and practicability standpoints.

FIG. 2 schematically illustrates a neurocomputer 50 according to principles of the
20 present invention. Neurocomputer 50 comprises a finite number n (in this case, $n=5$) oscillatory neural processing elements 60A, 60B, 60C, 60D and 60E. Elements 60A, 60B, 60C, 60D and 60E can comprise voltage-controlled oscillators, optical oscillators, lasers, microelectromechanical systems, Josephson junctions, macromolecules, or any other suitable oscillator known in the art. Each element 60A, 60B, 60C, 60D and 60E
25 oscillates at a particular frequency that may or may not be the same frequency as that of

the others of elements 60A, 60B, 60C, 60D and 60E. In its most general sense, the neurocomputer 50 further comprises a medium 70 connected to each of elements 60A, 60B, 60C, 60D and 60E by means of connective junctions 80A, 80B, 80C, 80D and 80E, respectively. Medium 70 may comprise a unitary body or multiple connected bodies.

- 5 Neurocomputer 50 further comprises a rhythmic forcing signal source 90 able to apply a modulated oscillatory frequency to medium 70 by means of a connection 100. Specifically, the medium 70 can be a conductive medium electrically connected to the oscillators 60A, 60B, 60C, 60D and 60E by conductive connection junctions 80A, 80B, 80C, 80D and 80E. The rhythmic forcing signal source 90 can be an electrical signal
- 10 generator such as a frequency modulated transmitter connected by a conductive connection 100 to the medium 70.

- In operation, any two elements, such as 60B and 60E, can be said to communicate to each other if changing the phase deviation of one influences the phase deviation of the other. Such is the case if the two elements oscillate at the same
- 15 frequency. Accordingly, if elements 60B and 60E oscillate at the same frequency, they will communicate in such manner.

- If elements 60B and 60E oscillate at different frequencies, they will not communicate in such manner. However, by causing input signal source 90 to apply a uniform oscillatory signal multiplicatively to elements 60A, 60B, 60C, 60D and 60E by
- 20 way of medium 70, any two oscillators, such as 60B and 60E, can be made to communicate by filling the frequency gap between them. That is, the uniform oscillatory signal must include a frequency equal to the difference between the respective frequencies of elements 60B and 60E. Accordingly, if elements 60B and 60E are oscillating at two different frequencies, say ω_1 and ω_2 , then applying the time (t)

dependent voltage signal $a(t)=\cos(\omega_1-\omega_2)t$ to medium 70 enables elements 60B and 60E to communicate data to each other.

Mathematical analysis of the said neurocomputer architecture, which is based on the theory developed by F. C. Hoppensteadt and E. M. Izhikevich (Oscillatory
5 neurocomputers with dynamic connectivity, Physical Review Letters 82(1999)2983-2986) shows that the neurocomputer dynamic is equivalent to a fully connected Hopfield network (J.J. Hopfield, Neural networks and physical systems with emergent collective computational abilities, Proceedings of National Academy of Sciences (USA) 79(1982)2554-2558). In particular, we use the well-known Hebbian learning rule
10 (D.O.Hebb, The Organization of Behavior, J. Wiley, New York, 1949; and S. Grossberg, Non-linear neural networks: Principles, mechanisms and architectures, Neural Networks 1(1988)17-61) to show that a network of $n = 60$ oscillators can memorize and successfully retrieve through associative recall three patterns corresponding to the images "0", "1", "2", as we illustrate in Figure 3. Thus, the neurocomputer can act as a
15 classical fully connected Hopfield network despite the fact that it has only n interconnections.

As discussed below, a neurocomputer according to principles of the present invention may be comprised mainly of phase-locked loops, amplifiers, and band-pass filters. A schematic of such a neurocomputer is shown in FIG. 8. In this discussion,
20 emphasis will be placed on the operation of phase-locked loops, which are ideally designed to perform frequency demodulation and frequency multiplication. Because of these qualities, they are highly suited for simulating neuron interaction.

A schematic of the major components of a phase locked loop ("PLL") 110 is shown in FIG. 4. The major components include a phase detector 120, low-pass filter 130, unity amplifier 140, and a voltage controlled oscillator ("VCO") 150. Phase locked loops use a feedback loop to produce a replica of an input signal's frequency. They are similar to operational amplifiers ("op-amps") in that an op-amp amplifies the voltage difference between input signals. The difference is that a PLL amplifies the frequency difference of the inputs and sets them equal to each other, so that the internally generated signal in the VCO 150 is an exact replica of the input signal (pin 4 of the PLL). Once this has occurred the PLL 110 is said to be in the "locked on" state. When the two signals are "locked on," any change in the input's frequency is detected by the phase detector 120 as an error signal. This error signal is applied to the internal signal, which is a replica of the input, so that it will match the input signal's frequency. The error signal is essentially the phase difference in the signal, which is the information waveform. The encoded information is extracted from pin 7 of the PLL 110. By implementing the above technique, frequency demodulation is performed using PLLs.

PLLs may be set up to perform frequency multiplication. This is accomplished by placing an open circuit between pins 3 and 4 in FIG. 4 and inputting a second source at pin 3. Since the phase detector 120 of PLL 110 is classified as type 1, it has a highly linear XOR gate and a built-in four-quadrant multiplier. The four-quadrant multiplier allows PLL 110 to perform frequency multiplication very accurately. A PLL connected in this manner produces an output that is the frequency multiplication of the two inputs.

Before simulating neuron activity using phase locked loop circuitry, one first establishes the free running frequency, the capture-range, and the lock-range of the PLL.

The free running frequency (f_0) is ideally the center frequency level of the signal that is to be demodulated. The value for the free running frequency is obtained from

$$f_0 = 1.2/(4 \bullet R1 \bullet C1) \quad (i)$$

It should be mentioned that the resistance R1 and the capacitance C1 correspond to the values of resistor R1 and capacitor C1 in FIG. 4. The capture-range (f_c) is the frequency range over which the PLL will try to lock on to an input's frequency. The following formula may be used to determine the capture-range.

$$f_c = 1/(2 \bullet \pi) \bullet \sqrt{((2 \bullet \pi \bullet f_L)/(3.6 \bullet 1000 \bullet C2))} \quad (ii)$$

where C2 is the capacitance of the similarly designated capacitor in FIG. 5 and f_L is the lock-range.

By evaluating the formula for the capture range, one can see that the capture range is limited by low pass filter time constant. The lock-range (f_L) is the range over which the PLL will remain in the locked on state. This range is generally larger than the capture-range and can be increased by increasing V_{cc} of the PLL as shown in the following equation.

$$f_L = 8 \bullet f_0 / V_{cc} \quad (iii)$$

After establishing the free running, lock and capture frequencies, it should be determined if there exists a linear relationship between the input frequency and phase, and the demodulated output voltage. This linear relationship can be determined and demonstrated as shown in FIG. 5.

Communication can occur when a signal is outside the capture range if it is conditioned by another signal. This can be demonstrated by implementing the multiple

PLL circuit 170 as shown in FIG. 6. The key to designing the circuit depicted in FIG. 6 is the ability to obtain the sum and difference of two input frequencies, which can be accomplished through multiplication.

In order to implement the multiplication operation as shown by the multiplication circle 171 or 172, one should understand the following theory:

$$\cos(\omega_c) \cos(\omega_m) = (1/2) \bullet [\cos(\omega_c - \omega_m) + \cos(\omega_c + \omega_m)]$$

$$\Rightarrow \text{Fourier Transform} \Rightarrow$$

$$(1/4) \bullet [\delta(f + (f_c - f_m)) + \delta(f + (f_c + f_m)) + \delta(f - (f_c - f_m)) + \delta(f - (f_c + f_m))]$$

FIG. 7 shows what occurs when multiplying 8kHz and 42kHz, as at the multiplier 171 in FIG. 7. As seen in FIG. 8, these 8kHz and 42kHz components are present in the output 172 of the multiplier 171. Also present are 50kHz and 34 kHz, the sum and difference of 8 kHz and 42 kHz, respectively. Interfering harmonics are also present. Here, 8 kHz and 42 kHz were chosen to obtain an adequate separation between the harmonics and the desired frequency components.

To resolve the problem of harmonic frequencies output by the multipliers 171, 173, band pass filters were placed in the circuit. The filter was comprised of an inductor and capacitor. To isolate the single frequency desired, the following formula was used:

$$f = 1/(\sqrt{L \bullet C \bullet 2 \bullet \pi}) \quad (iv)$$

This formula was used to choose the desired inductor and capacitor needed. A problem resulting from the addition of the band pass filter was a voltage drop of the input signal. To compensate for this drop, amplifiers were inserted into the circuit to raise the voltage

back up to the desired magnitude. The band pass filter amplifier circuits thus added are indicated at 175, 176 of FIG. 6.

By modulating the 8 kHz carrier frequency of the function generator 178 with a 100 Hz sine wave modulation and multiplying the modulated signal with a 42 kHz carrier frequency, the PLL 181 was able to demodulate the input signal and output the 100 Hz information signal. Similarly, the PLL 182 was able to demodulate the 100 Hz information signal. Testing of the circuit depicted in FIG. 6 demonstrates that communication can still occur even if a signal is outside the capture range of a PLL if the information signal is combined with another carrier signal.

In FIG. 8, the circuit shown in block diagram form in FIG. 6 is schematically shown in greater detail. The multipliers 172 and 173 are LM 565 phase locked loops from National Semiconductor. National Semiconductor op amps LM 324 are used in the band pass filter and amplification stages 175 and 176 along with the inductor and capacitor filtering circuit elements of the values shown. The phase locked loops 181 and 182 connected as oscillators employ the LM 565 phase locked loops from National Semiconductor. VCC_1 , from the PLL oscillator 181 at the upper right, is fed back to the multiplier 173 at the lower left and VCC_2 is fed back from the PLL oscillator 182 at the lower right to the multiplier 172 at the upper left.

In FIG. 9, a five-element neural network 190 is shown. Five phase locked loop oscillators 191, 192, 193, 194 and 195 are tuned at frequencies W_1, W_2, W_3, W_4, W_5 , respectively, where the ratio of frequencies is $W_1:W_2:W_3:W_4:W_5 = 1:2:3:4:5$. These oscillators are forced by a common function generator 198. The function generator is connected to the oscillators via the conductors 200 and 202 serving as the conductive medium and connectors, respectively, of the neural network 190 previously discussed.

Oscilloscopes 211, 212, 213, 214, and 215 are connected to the oscillators as illustrated to demonstrate the output signals of the oscillators responsive to various inputs from the function generator 198. A summing circuit 217 is connected into a feedback loop 218 common to each of the oscillators.

5 FIGS. 10-13 illustrate the responses of the oscillators 191-195, respectively, to four input signals generated by the function generator 198. FIG. 10 shows the traces of the oscilloscopes 211-215 corresponding to the oscillating signals of oscillators 191-195, respectively, when the forcing voltage from the function generator 198 is $\sin t$. None of the oscillators 191-195 are in communication and the oscillator signals are unrelated, as
10 shown by the traces 10A-10E.

 With a function generator input $\sin 2t$, the oscillators respond with signals as shown by the traces of FIGS. 11A to 11E. Here, the oscillators 191, 193 and 195 communicate, producing the oscilloscope traces of FIGS. 11A, 11C and 11E, and the oscillators 192 and 194 communicate producing the traces of FIGS. 11B and 11D.

15 With an input signal $\sin 3t$ impressed by the function generator 198, the oscillators 191-195 produce in the oscilloscopes 211-215 the traces shown at FIGS. 12A-12E, respectively. Oscillators 191 and 194 communicate, producing the traces of FIGS. 12A and 12D. Oscillators 192 and 195 communicate producing the traces shown at FIGS. 12B and 12E. The oscillator 193 is not in communication with any other of the
20 oscillators and it produces the trace shown at FIG. 12C.

 In FIGS. 13A-13E, shown are traces illustrating the response of the oscillators 191-195 when a signal $\sin 10t$ is impressed by the function generator 198. None of the oscillators here are communicating.

A further, more generalized example of implementation of the present invention will now be described using a network of n voltage controlled oscillators (known as Kuramoto's phase model) and represented by:

$$\dot{\vartheta}_i = \Omega_i + \varepsilon a(t) \sum_{j=1} \sin(\vartheta_j - \vartheta_i), \quad (1)$$

where $\vartheta_i \in S^1$ is the phase of the i th oscillator, $a(t)$ is the external input and $\varepsilon \ll 1$ is the strength of connections. We require that all differences $\Omega_i - \Omega_j$ be different when $i \neq j$.

(i) Averaging

Let $\vartheta_i(t) = \Omega_i t + \varphi_i$, then

$$\dot{\varphi}_i = \varepsilon a(t) \sum_{j=1}^n \sin(\{\Omega_j - \Omega_i\}t + \varphi_j - \varphi_i). \quad (2)$$

One can average this system to obtain

$$\dot{\varphi}_i = \varepsilon H_i(\varphi_1, \dots, \varphi_n) + o(\varepsilon), \quad (3)$$

where

$$H_i = \lim_{T \rightarrow \infty} \frac{1}{T} \int_0^T a(t) \sum_{j=1}^n \sin(\{\Omega_j - \Omega_i\}t + \varphi_j - \varphi_i) dt$$

5 is the average of the right-hand side of (2).

(ii) Quasiperiodic External Input

Now suppose we are given a matrix of connections $C = (c_{ij})$. Let

10

$$a_i(t) = a_c + \sum_{j=1}^n \sum_{l=1}^n c_{lj} \cos(\{\Omega_j - \Omega_l\}t) \quad (4)$$

be a time dependent external input, which is a quasiperiodic function of t . Since all $\Omega_j - \Omega_i$ differences are different for all i and j , it is easy to verify that

$$H_i = \sum_{j=1}^n \frac{c_{ij} + c_{ji}}{2} \sin(\varphi_j - \varphi_i)$$

If we denote $s_{ij} = (c_{ij} + c_{ji})/2$, use the slow time $\tau = \epsilon t$, and disregard the small-order
20 term $o(\epsilon)$, then we can rewrite system (2) in the form

$$\varphi_i' = \sum_{j=1}^n s_{ij} \sin(\varphi_j - \varphi_i), \quad (5)$$

where $\dot{\tau} = d\tau/dt$. We see that the external input of the form (4) can dynamically connect any two oscillators provided that the corresponding c_{ij} is not zero.

5 (iii) Chaotic External Input

In general, the external input $a(t)$ can be chaotic or noisy. It can dynamically connect the i th and the j th oscillators if its Fourier transform has a non-zero entry corresponding to the frequency $\omega = \Omega_j - \Omega_i$ since the average, H_i , would depend on the phase difference

10 $\varphi_j - \varphi_i$ in this case.

(iv) Oscillatory Associative Memory

Since the connection matrix $S = (s_{ij})$ is symmetric, the phase model (5) is a gradient

15 system. Indeed, it can be written in the form

$$\dot{\varphi}_i = -\frac{\partial U}{\partial \varphi_i}$$

where

20

$$U(\varphi_1, \dots, \varphi_n) = -\frac{1}{2} \sum_{i=1}^n \sum_{j=1}^n s_{ij} \cos(\varphi_j - \varphi_i)$$

is a gradient function. The vector of phase deviations $\varphi = (\varphi_1, \dots, \varphi_n) \in \mathbb{T}^n$ always converges to an equilibrium on the n -torus $\in \mathbb{T}^n$ as shown in FIG. 3. System (5) has multiple attractors and Hopfield-Grossberg-like associative properties as also shown in FIG. 3. Therefore, system (1) with external forcing has oscillatory associative memory.

5

(v) Hebbian Learning Rule

Suppose we are given a set of m key vectors to be memorized

10

$$\xi^k = (\xi_1^k, \xi_2^k, \dots, \xi_n^k), \quad \xi_i^k = \pm 1, \quad k = 1, \dots, m,$$

where $\xi_i^k = \xi_j^k$ means that the i th and the j th oscillators are in-phase ($\varphi_i = \varphi_j$), and

$\xi_i^k = -\xi_j^k$ means they are anti-phase ($\varphi_i = \varphi_j + \pi$). A Hebbian learning rule of the form

$$s_{ij} = \frac{1}{n} \sum_{k=1}^m \xi_i^k \xi_j^k, \quad (6)$$

15

is the simplest one among many possible learning algorithms. To get (5) it suffices to apply the external input of the form (4) with $c_{ij} = s_{ij}$ for all i and j .

(vi) Initializing the Network

20

To use the proposed neurocomputer architecture to implement the standard Hopfield-Grossberg paradigm, as we illustrate in FIG. 3, we need a way to present an input image as an initial condition $\varphi^{(0)}$, and to read the output from the network. While the latter

task poses no difficulty and can be accomplished using Fourier analysis of the "mean field activity," the former task requires some ingenuity since we do not have direct access to the oscillators.

Suppose we are given a vector $\xi^0 \in \mathbb{R}^n$ to be recognized. Let us apply the external input $a(t) \quad c_{ij} = \xi_i^0 \xi_j^0$ with for a certain period of time. This results in the phase deviation system of the form

10

$$\dot{\varphi}_i = \sum_{j=1}^n \xi_i^0 \xi_j^0 \sin(\varphi_j - \varphi_i)$$

It is easy to check that if, $\xi_i^0 \xi_j^0 = 1$ then $\varphi_i(t) - \varphi_j(t) \rightarrow 0$. and if $\xi_i^0 \xi_j^0 = -1$ then

15 $\varphi_i(t) - \varphi_j(t) \rightarrow \pi$ for all i and j . Thus, the network activity converges to the equilibrium having phase relations defined by the vector ξ^0 , as shown in FIG. 3. When we restore the original external input $a(t)$, which induces the desired dynamic connectivity, the recognition starts from the input image ξ^0 . (We added noise to the image ξ^0 shown in FIG. 3 to enhance the effect of convergence to an attractor during recognition.)

20 Although the invention has been described in terms of the illustrative embodiment, it will be appreciated by those skilled in the art that various changes and modifications may be made to the illustrative embodiment without departing from the spirit or scope of the invention. It is intended that the scope of the invention not be limited in any way to the illustrative embodiment shown and described but that the

25 invention be limited only by the claims appended hereto.

WHAT IS CLAIMED IS:

1. A neurocomputer comprising:
 - a plurality of n processing elements;
 - a plurality of connectors operably coupled with said elements;
 - 5 a conductive medium operably coupled with said connectors; and
 - a forcing apparatus operably coupled with said medium.
2. The neurocomputer of claim 1, wherein:
 - said plurality of connectors comprises no more than n connectors,
 - each of
 - 10 said connectors being operably coupled with a corresponding one of said elements.
3. The neurocomputer of claim 1, wherein:
 - said forcing apparatus comprises a rhythmic input.
4. The neurocomputer of claim 1, wherein:
 - said elements comprise oscillators.
- 15 5. A neurocomputer comprising:
 - a plurality of n oscillating processing elements;
 - a plurality of no more than n connectors, each of said connectors
 - being operably coupled with a corresponding one of said elements;
 - a conductive medium operably coupled with said connectors; and
 - 20 a rhythmic input operably coupled with said medium.
6. A neurocomputer comprising:
 - a plurality of n processing element means;
 - a plurality of connectors operably coupled with said element
 - means;

means for simultaneously applying an oscillatory signal to each of
said element means via said connectors; and

means for generating said oscillatory signal operably coupled with
said means for applying.

5 7. The neurocomputer of claim 6, wherein:

 said plurality of connectors comprises n connectors, each of said
connectors being operably coupled with a corresponding one of said element means.

 8. The neurocomputer of claim 6, wherein:

 said element means comprise oscillators.

10 9. The neurocomputer of claim 6, wherein:

 said means for applying comprises a conductive medium.

 10. The neurocomputer of claim 6, wherein:

 said means for generating comprises a rhythmic input.

 11. An oscillatory neurocomputer comprising:

15 a number n of oscillating elements
 a source of a rhythmic forcing input,
 a medium interconnecting the source of rhythmic forcing input to
 each
oscillating element,

20 each oscillating element having an oscillating frequency,
 the oscillating frequency f_1 of at least one of the oscillating
elements differing from the oscillating frequency f_2 of at least one other of the oscillating
elements,

the source of a rhythmic forcing input producing an input of a third frequency f_3 , establishing communication between the at least one oscillating element and the at least one other oscillating element.

12. An oscillatory neurocomputer according to claim 11, wherein f_3 is
5 substantially the difference between f_1 and f_2 .

13. An oscillatory neurocomputer according to claim 11, further comprising a number n_1 of connections of the source of a rhythmic forcing input to the oscillating elements, wherein

$$n_1 \leq n.$$

- 10 14. An oscillatory neurocomputer according to claim 12, further comprising a number n_1 of connections of the source of a rhythmic forcing input to the oscillating elements, wherein

$$n_1 \leq n.$$

- 15 15. An oscillatory neurocomputer according to claim 11, wherein the oscillating elements are electronic oscillators, the source of a rhythmic forcing input is a function generator and the interconnecting medium is an electrically conductive medium electrically connecting the source of a rhythmic forcing input to the oscillators.

16. An oscillatory neurocomputer according to claim 15, wherein the function generator provides a forcing signal having a carrier frequency and information content
20 modulating the carrier frequency, the oscillators responding to the impression of the forcing signal onto the conductive medium to produce information content modulation substantially the same as that of the conductive medium.

17. An oscillatory neurocomputer according to claim 11, wherein the number
n of

oscillating elements is greater than two, a first subset of the oscillating elements communicate at a frequency f_3 of rhythmic forcing input from the source, and at least one second subset of the oscillating elements communicate at least one further frequency f_4 of rhythmic forcing input from the source.

- 5 18. An oscillatory neurocomputer according to claim 15, wherein content
 varying one

oscillator from its oscillating frequency is communicated to and varies from its
oscillating frequency another oscillator in communication with the one oscillator.

19. A neurocomputer including:

- 10 (a) an array of oscillators, at least a plurality of said oscillators having
 differing frequencies,

- (b) a common conducting medium connected to each of the plurality
 of

oscillators,

- 15 (c) a source connected to the conducting medium to impart oscillator
 signals

of various frequencies to the conducting medium, the signals of various frequencies
including frequencies effective to bring two or more of the oscillators into
communication.

- 20 20. An oscillatory neurocomputer according to claim 19, wherein the
 oscillators include feedback circuits connected with the medium.

 21. An oscillatory neurocomputer according to claim 20, wherein the
 oscillators are phase locked loops.

22. A method of enabling communication of a characteristic between a first processing element oscillating at a first frequency and a second processing element oscillating at a second frequency different from the first frequency, the method comprising the steps of:

- 5 operably coupling the first element to a medium;
operably coupling the second element to said medium;
operably coupling said medium to a rhythmic input; and
causing said rhythmic input to oscillate said medium at a third frequency.

- 10 23. The method of claim 22, wherein:
said third frequency comprises a frequency substantially equal to
the
difference between the first frequency and the second frequency.

24. A method of enabling communication of a characteristic between a
15 plurality of n oscillating processing elements comprising the steps of:

- operably coupling each of the plurality of n elements to a
corresponding one of a plurality of no more than n connectors;
operably coupling each one of said connectors to a conductive
medium; and
20 operably coupling said medium to a rhythmic input.

25. In a neurocomputer, a number n of active elements and a medium having connections to the active elements for application of an input signal thereto, said active elements being phase locked loop oscillators.

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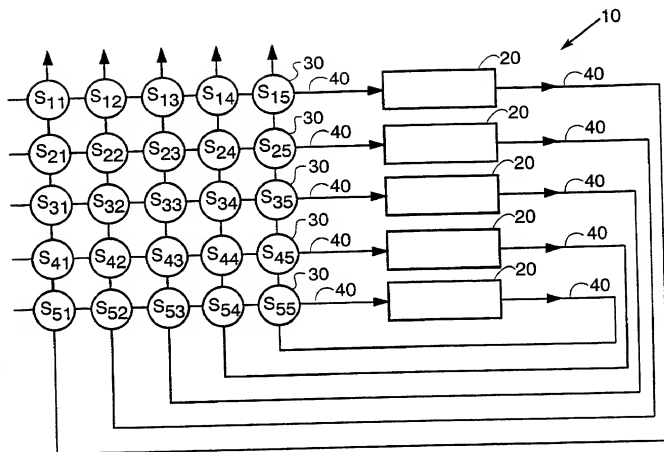


FIG. 1.
(PRIOR ART)

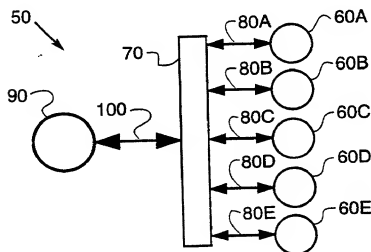


FIG. 2.

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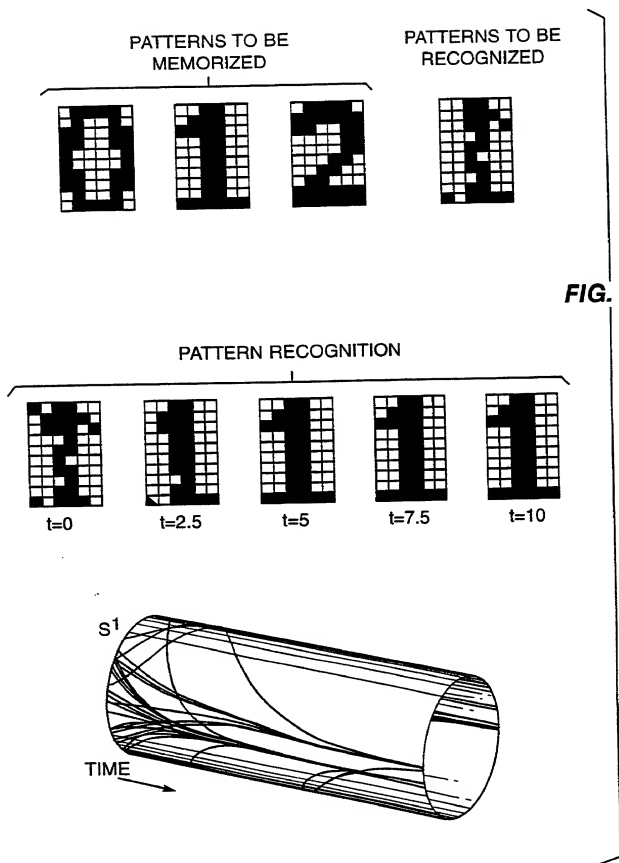


FIG. 3.

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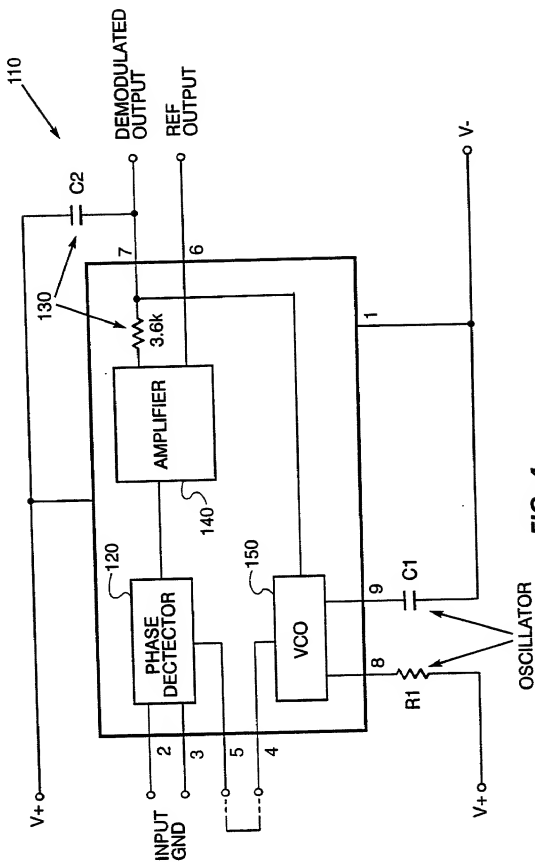
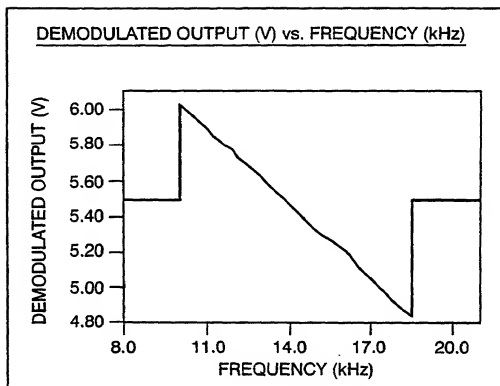


FIG. 4.

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**FIG. 5.**

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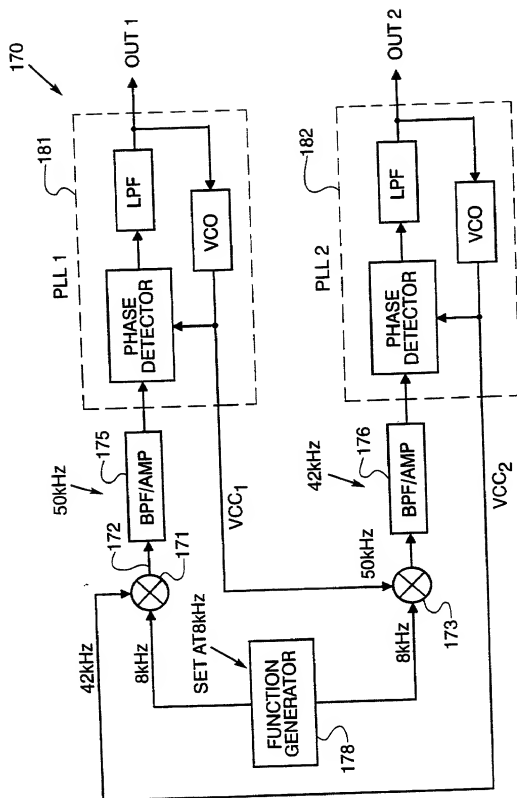
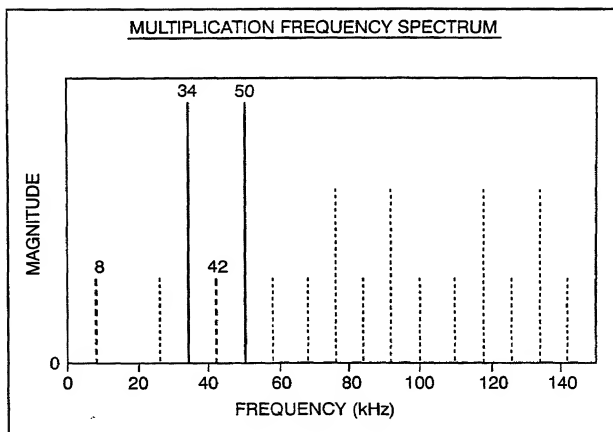


FIG. 6.

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**FIG. 7.**



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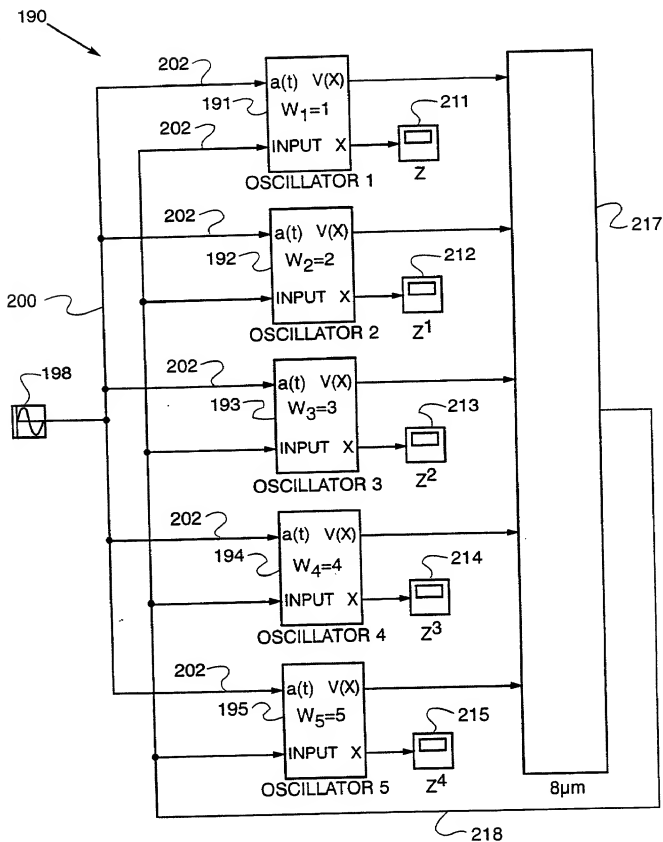
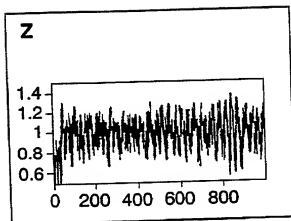
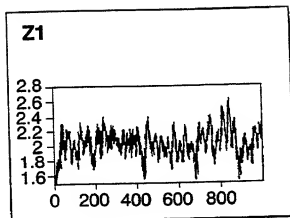
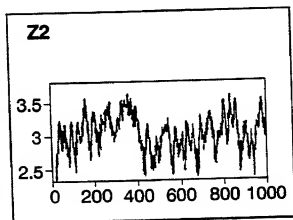
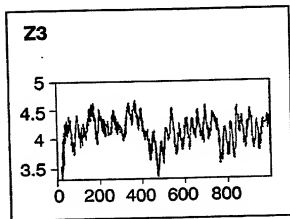
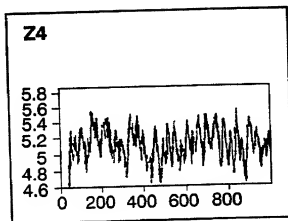
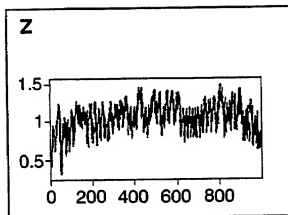
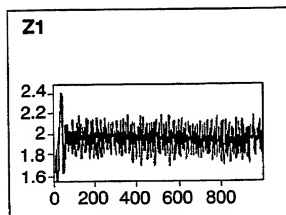
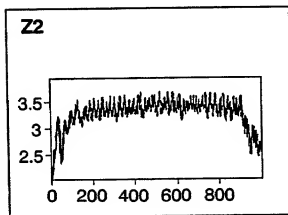
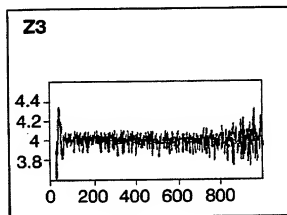
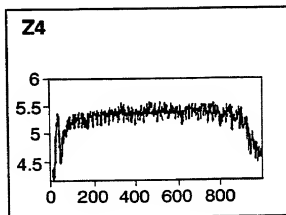


FIG. 9.

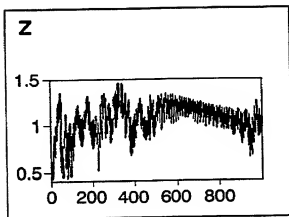
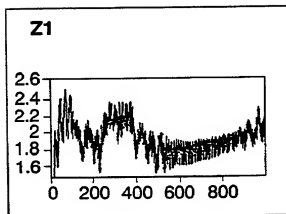
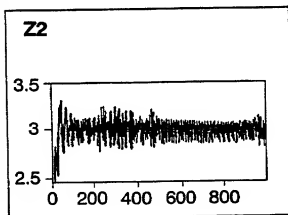
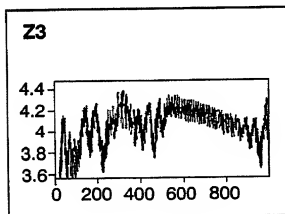
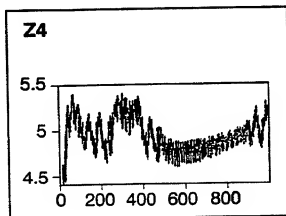
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**FIG. 10A.****FIG. 10B.****FIG. 10C.****FIG. 10D.****FIG. 10E.**

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**FIG. 11A.****FIG. 11B.****FIG. 11C.****FIG. 11D.****FIG. 11E.**

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**FIG. 12A.****FIG. 12B.****FIG. 12C.****FIG. 12D.****FIG. 12E.**

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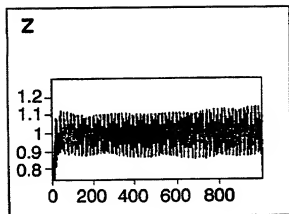


FIG. 13A.

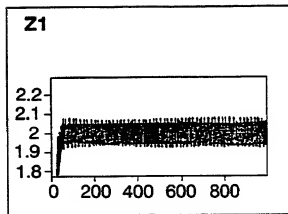


FIG. 13B.

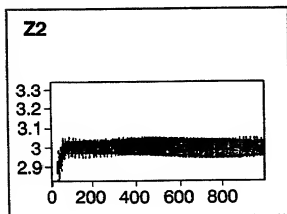


FIG. 13C.

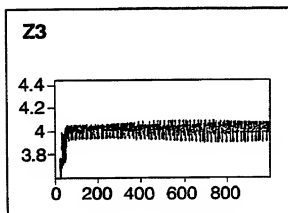


FIG. 13D.

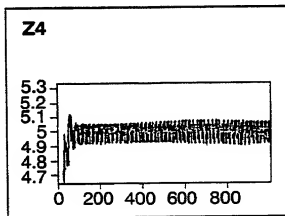


FIG. 13E.

**COMBINED DECLARATION
AND POWER OF ATTORNEY**

(Original, Design, National Stage of PCT or CIP Application)

As below named inventors, We hereby declare that:
Our residence, post office address and citizenship are as stated below next to our names; We believe We are the original, first and sole inventors (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

OSCILLATORY NEUROCOMPUTERS WITH DYNAMIC CONNECTIVITY

the specification of which: (complete (a), (b) or (c) for type of application)

Regular or Design Application

- (a) ☐ is attached hereto.
(b) ☐ was filed on _____ as Application Serial No. _____ and as amended on _____ (if applicable).

PCT Filed Application Entering National Stage

- (c) ☒ was described and claimed in International Application No. PCT/US99/26698 filed on November 12, 1999 and as amended on _____ (if applicable).

Acknowledgment of Review of Papers and Duty of Candor

We hereby state that We have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

We acknowledge the duty to disclose information which is material to the patentability of the subject matter claimed in this application in accordance with Title 37, Code of Federal Regulations § 1.56.

☐ In compliance with this duty there is attached an information disclosure statement. 37 CFR 1.97.

Priority Claim

We hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed

(complete (d) or (e))

(d) [X] no such applications have been filed.

(e) [] such applications have been filed as follows:

PRIOR FOREIGN/PCT APPLICATION(S) FILED WITHIN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO SAID APPLICATION				
COUNTRY	APPLICATION NO.	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)	PRIORITY CLAIMED UNDER 37 USC 119
				[] YES NO []
				[] YES NO []
				[] YES NO []
ALL FOREIGN APPLICATION(S), IF ANY, FILED MORE THAN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO SAID APPLICATION				
				[] YES NO []

Claim for Benefit of Prior U.S. Provisional Application(s)

We hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

Provisional Application Number	Filing Date
60/108,353 /	November 13, 1998
/	
/	

Continuation-In-Part

(complete this part only if this is a continuation-in-part application)

We hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code § 112, I acknowledge the duty to disclose information as defined in Title 37, Code of Federal Regulations, § 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status)	(patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status)	(patented, pending, abandoned)

Power of Attorney

As named inventors, We hereby appoint Thomas D. MacBlain, Reg. No. 24,583, Kittie Murray, Reg. No. 30,346, John Titus, Reg. No. 39,047, Paul Burns, Reg. No. P47,463, and Rennie Dover, Reg. No. 36,503, of the firm of GALLAGHER & KENNEDY, with offices at 2575 East Camelback Road, Phoenix, Arizona 85016 as attorneys and agents to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

SEND CORRESPONDENCE TO:

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We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FULL NAME OF SOLE OR FIRST INVENTOR	LAST NAME <u>Hoppensteadt</u>	FIRST NAME <u>Frank</u>	MIDDLE NAME <u>C.</u>
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DATE <u>7/16/01</u>	SIGNATURE OF INVENTOR <i>[Signature]</i>		ZIP CODE <u>85253</u>
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FULL NAME OF THIRD JOINT INVENTOR, IF ANY	LAST NAME	FIRST NAME	MIDDLE NAME
RESIDENCE & CITIZENSHIP	CITY	STATE or FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP
POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE or COUNTRY ZIP CODE
DATE	SIGNATURE OF INVENTOR		